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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,374	11/13/2003	Rajen Chanchani	SD7151/S98758	1623

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,374	CHANCHANI, RAJEN	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *13-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/713374 Attorney's Docket #:SD7151/S98758
Filing Date: 11/13/12003;

Applicant: Chanchani

Examiner: Alexander Williams

Applicant's election of Group I (claims 1 to 12), filed 9/27/05, has been acknowledged.

This application contains claims 13 to 16 drawn to an invention non-elected without traverse.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The use of the trademark all thru the specification has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 12 are rejected under 35 U.S.C. § 102(e) as being anticipated by Forcier (U.S. Patent # 6,919,508 B2).

1. Forcier (figures 5 to 13) specifically figures 7 and 8 show a microsystem-on-a-chip, comprising: a bottom chip **850** comprising one or more microsystem devices **840** with associated input/output pads on the top surface of the bottom chip; an interconnect layer **(within 830)** on the top surface of the bottom chip, the interconnect layer comprising a compliant dielectric material **830** and an interconnect structure embedded in the compliant dielectric material, the interconnect structure comprising one or more via capture pads connected to the associated input/output pads on the top surface of the bottom chip; and a thin upper chip **800,860** on the interconnect layer, the thin upper chip comprising one or more microsystem devices with associated input/output pads on

the top surface of the thin upper chip that are connected to the one or more via capture pads in the interconnect layer by conductive vies through the thin upper chip.

[0009] Complex build-up on die processing suffers from technological constraints due to reliability and quality issues when temperature excursions (as in soldering) cause fractures in the composite which are due to Coefficient of Thermal Expansion (CTE) differences between the various materials and components of the package. These issues are even more problematic when attempts are made to package multiple die of different geometries and materials in a monolithic structure. For example, encapsulation materials of the embedded die and the design of the vias often result in an undesirably rigid structure which, combined with the CTE mismatch materials, causes delamination (adhesion failure) during a thermal stress or soldering operation. Furthermore, the embedding of various components, such as sensors, MEMs (Micro Electromechnaical Machines), capacitors, resistors, inductors, transducers and antennas, each of which typically has a unique CTE, cannot be performed in multicomponent structures due to additional stress issues of the various materials and their different CTE values.

[0014] Typically, build-up on die and chip scale packaging utilize **copper** vias with various configurations such as plated-through-holes, blind vias, buried vias, or microvias for interconnecting the die and the copper circuitry in a package. These vias connect one circuitry layer (sometimes referred to as metal layer) to the next. These vias are usually formed 90 degrees to the plane of the circuitry, die, or **dielectrics**.

[0022] The embodiments of the present invention described herein make use of a stud bumping process for preparation of die interconnect pads and also two methods of **dielectric** application to a wafer or singular die: a) spin coating and b) press lamination. The stud bumping process has been demonstrated in die form. A typical stud bumping process machine is provided by a model 8098 Large Area Ball Bonder by Kulicke and Soffa. Stud bump wire is typically gold wire, although copper, solder, non-lead solder alloys and various other materials may be used without departing from the spirit or the scope of the invention. Spin coating and press lamination have been demonstrated for a 6" diameter wafer. Typical dielectrics for a build-up process as implemented in the present invention include nanocomposites, mesocomposites, and mesoporous materials such as those provided

by SBA Materials, Inc. in Santa Barbara, Calif., also referred to as self-assembled inorganic/block-copolymer composites and mesoporous solids. Flexible Circuit materials and adhesives are preferably similar to Dupont's Pyralux system. Very High Tg organic polymers are preferably used, such as Sumitomo's PolyBenzoxazole (PBO) 8000 series, which has a Tg of approximately 300C; Dow Chemical's BenzoCycloButene (BCB), which has a Tg of approximately 300C; HD Microsystems' (Joint venture Dupont/Hitachi) Polyimide (PIQ, PIX tradenames), which has a Tg greater than 300C; or Brewer Science Inc.'s polyimide photoimageable dielectrics. Thermally conductive adhesives and films used herein are preferably similar to Ablefilm 561K. Epoxy coated copper as used herein is preferably similar to Oak-Mitsui Coated Copper. Anisotropic conductive films used herein are preferably of a type similar to ACF from ITO America and a product of the Sony Corporation. **Embedded passive materials** used herein are preferably similar to high Dk 25 micron film laminates from 3M or Oak-Mitsui. Laser Machining has been and will be utilized in this process using equipment such as, without limitation, the ESI Model 5430 UV Laser Microvia drilling machine. Solder sphere placement for interconnection has been implemented with equipment such as Shibuya's SolderBall Mounter Model SBM360. Sputtering of copper metal for interconnects has been implemented with equipment such as SFI Metal Depositor Model 8600. Microlithograph has been performed with Spectrum 3 Ultratech Steppers. Dielectric Placement has been performed with spin coaters such as Karl Suss Model ACS-200 and anisotropic film bonders similar to those distributed by Ito America. The above-referenced materials and equipment are included herein as exemplary of those used in a preferred embodiment of the present invention, and should not be interpreted as limiting the scope of the invention thereto. It should be apparent to one skilled in the art that alternative materials and equipment may be substituted therefor without departing from the spirit or the scope of the invention.

[0040] A build-up electrical structure that is fabricated with a build-up process and multi-angle vias for interconnecting die or multiple die and/or passive components such as capacitors, Microelectromechanical Machines (MEMs), Nanoelectromechanical Machines (MEMs), Bioelectromechanical Machines (BioMEMs), sensors, planar capacitors, resistors, planar resistors, inductors, fuel cells, antennas, thin film batteries, VCSEL's, photodiodes, **or other active** and passive **components** is described

herein. Typical preferred process times and temperatures are 350.degree. C. for one hour with normal prepregs, 250.degree. C. for 90 seconds with mesoporous materials and 350.degree. C. for 20 seconds for anistropic conductive adhesives. Typical process temperatures for very high Tg photo-imageable dielectrics would be 375.degree. C. for 1 hour. Via formations are preferably made with laser milling with an ultraviolet or carbon dioxide laser, although via formations can be made using a photolithography process followed by developing and/or chemical milling, or with soft lithography. Stud Bumping preferably utilizes gold wire and is performed with a stud bumping machine such as the K&S 300 mm stud bumping machine. Chip placement is preferably performed with standard chip placement robotics with placement accuracies to 0.5 micron. The above-referenced process times, temperatures, and equipment are included herein as exemplary of those used in a preferred embodiment of the present invention, and should not be interpreted as limiting the scope of the invention thereto. It should be apparent to one skilled in the art that alternative process times, temperatures, and equipment may be substituted therefor without departing from the spirit or the scope of the invention.

[0041] FIG. 5 illustrates a build-up on die with multi-Angle Via Process and structure. Die or other active components such as MEMs 500 are tack-bonded into a multi-depth cavity 515 using a thermally conductive adhesive film 505 with a die bonding and placement machine. Multi-angle stud bumps 520 are placed on the active sites of the die and/or components in each of the active sites requiring interconnection. A controlled CTE dielectric 530, such as a mesoporous material or a very high Tg photo-imageable dielectric, is deposited over the die or multiple die utilizing a spin coating or lamination process thereby sandwiching and embedding the die. An optical waveguide is formed with the nanocomposites or nanoporous materials if required for chip to chip optical interconnects 535 and a dielectric channel 540 is formed to expose the stud bumping through soft lithography, photolithography or laser trenching. Copper plating 550 is deposited on the surface and in the channels utilizing either wet chemistry plating or sputtering. In a subsequent step, copper circuitry 560 is preferably etched in the copper plating utilizing photolithography and chemical milling, thereby forming a first circuitry (first metal) layer. Solder Mask 580 and solder balls 570 are placed on the structure surface utilizing sphere drop

equipment to complete the interconnect and to allow attachment to other interconnects. The multi-depth cavities accommodate different die thicknesses and the multi-angle vias allow for escape routing from the die to other components.

[0043] FIG. 7 illustrates another embodiment of the present invention. In this embodiment, a flex circuit substructure 700, with multi-angle vias 740, is fabricated with an optical waveguide of mesocomposite material 730 applied to the bottom side of the flex circuit substructure and positioned between the optical vias of the substructure. The multiangle vias allow light to transmit by reflection through the optical via. This structure forms an optical pathway from a VCSEL laser light source 710 on the surface to a photodiode 720, also on the surface with the light pathway following the multi-angle vias on either side of the optical waveguide. This flex circuit is then attached to a backplane multilayer 750 utilizing an adhesive film 745 with a lamination process and a plated-through hole process, thereby completing the optical and electrical interconnect.

[0044] FIG. 8 illustrates an electrical version of FIG. 7 with embedded die. A flex circuit 800 with multi-angle electrical vias 820 is laminated to a multilayer substrate 850 with anisotropic conductive adhesive 830. A completed multilayer substrate 860 is produced by finishing the structure with a standard printed circuit process to achieve plated-through holes. Electrical interconnection between components and die is accomplished through the anisotropic conductive adhesive and the multi-angle stud bumping and electrical vias.

2. The microsystem-on-a-chip of Claim 1, Forcier further comprising at least one additional stacked layer **810,800,860** on the thin chip, each additional stacked layer comprising: a stacked interconnect layer on the top surface of the thin upper chip, the stacked interconnect layer comprising a compliant dielectric material and an interconnect structure embedded in the compliant dielectric material, the interconnect structure comprising one or more via capture pads connected to the associated input/output pads on the top surface of the thin upper chip; and a stacked thin chip on the stacked interconnect layer, the stacked thin chip comprising one or more microsystem devices with associated input/output pads on the top surface of the

stacked thin chip that are connected to the one or more via capture pads in the stacked interconnect layer by conductive vies through the stacked thin chip.

3. The microsystem-on-a-chip of Claim 1, Forcier show wherein the interconnect layer has a thickness of less than 50 microns.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

4. The microsystem-on-a-chip of Claim 1, Forcier show wherein the compliant dielectric material is a polymer.

5. The microsystem-on-a-chip of Claim 4, Forcier show wherein the polymer is benzocyclobutene.

6. The microsystem-on-a-chip of Claim 1, Forcier show wherein the thin upper chip has a thickness of less than 120 microns.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

7. The microsystem-on-a-chip of Claim 1, Forcier show wherein the interconnect structure further comprises at least one passive component.

8. The rnicrosystem-on-a-chip of Claim 7, Forcier show wherein the embedded passive comprises a thin film resistor.

9. The microsystem-on-a-chip of Claim 7, Forcier show wherein the embedded passive comprises a multi-layer capacitor.

10. The microsystem-on-a-chip of Claim 7, Forcier show wherein the embedded passive comprises a spiral inductor.

11. The microsystem-on-a-chip of Claim 1, Forcier show wherein the interconnect structure comprises copper.

12. The microsystem-on-a-chip of Claim 1, Forcier show wherein the on or more via capture pads are sized to control the alignment tolerance of the thin upper chip.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,724,728,780,680,681,774,773,678, 679 174/52.4	11/5/05
Other Documentation: foreign patents and literature in 257/686,685,723,777,724,728,780,680,681,774,773,678, 679 174/52.4	11/5/05
Electronic data base(s): U.S. Patents	11/5/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
11/6/05